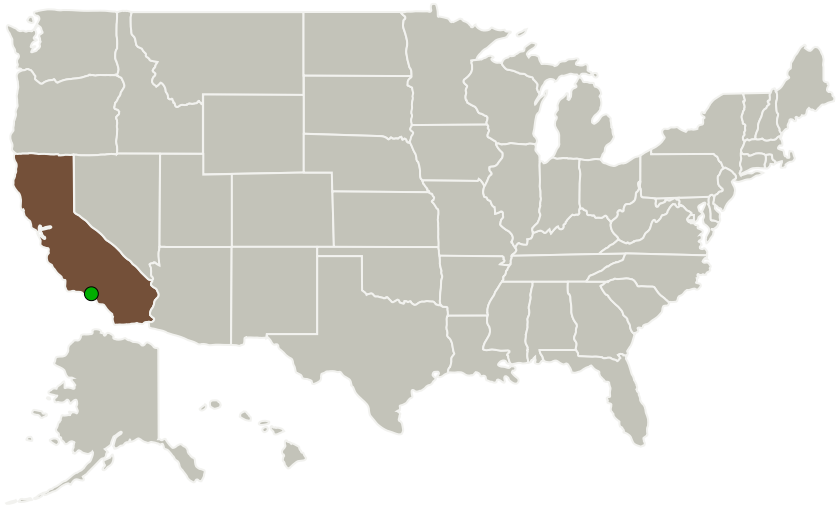
20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase I

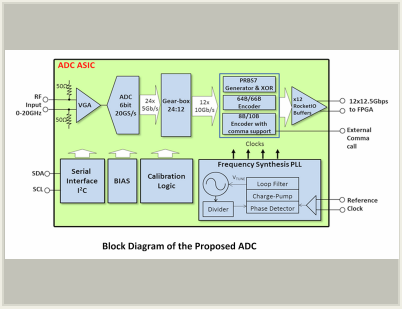
Completed Technology Project (2016 - 2016)

Project Introduction

The proposed project aims to develop a 20GSps 6-bit radiation hardened analog to digital converter (ADC) required for microwave radiometers being developed for space and air borne earth sensing applications. Aiming to improve performance and to reduce the size of the electronics, high resolution, high-sampling rate, power efficiency and low spur energy are the requirements for ADCs employed for direct digitization in microwave radiometers. The proposed 20GS/s 6-bit interleaved successive approximation (SAR) ADC is intended to achieve >5 ENOB and 20GHz input bandwidth. A number of innovations will be introduced to the ADC in order to combine low power consumption with high signal to noise and distortion (SINAD), and spurious free dynamic range (SFDR) which is important for spectrography applications. A novel low glitch energy technique coupled with interleaved samples aperture calibration will be introduced to achieve digitization accuracy, improve linearity and achieve high sampling rate. The proposed ADC ASIC will contain on-chip all necessary components, including a frequency synthesizer, serial interface, standard interface with an FPGA, and design-for-testability features. The ADC will be implemented using a deep submicron CMOS technology. The project's Phase I will provide the proof of feasibility of implementing the proposed ADC. Phase II will include finishing design, fabrication, testing and delivering the ADC prototypes which will be ready for commercialization in Phase III.

Primary U.S. Work Locations and Key Partners





Block Diagram of the Proposed ADC

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Table of Contents

Small Business Innovation Research/Small Business Tech Transfer

20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase I

Completed Technology Project (2016 - 2016)

Organizations Performing Work	Role	Type	Location
Pacific Microchip Corporation	Lead Organization	Industry	Culver City, California
Jet Propulsion Laboratory(JPL)	Supporting Organization	NASA Center	Pasadena, California

Primary U.S. Work Locations
California

Project Transitions

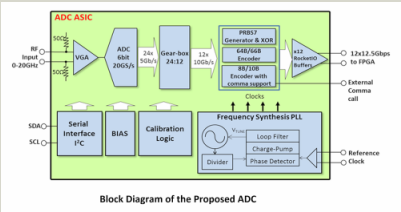
June 2016: Project Start

December 2016: Closed out

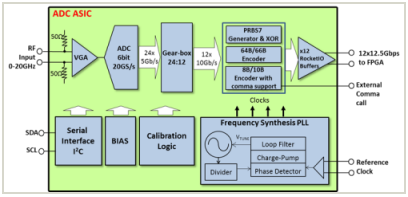
Closeout Documentation:

- Final Summary Chart*(https://techport.nasa.gov/file/139566)*

Images



Briefing Chart Image
20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase I *(https://techport.nasa.gov/image/128203)*



Final Summary Chart Image
20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase I Project Image *(https://techport.nasa.gov/image/128819)*

Organizational Responsibility

Responsible Mission Directorate:
Space Technology Mission Directorate (STMD)

Lead Organization:
Pacific Microchip Corporation

Responsible Program:
Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:
Jason L Kessler

Program Manager:
Carlos Torrez

Principal Investigator:
Denis Zelenin

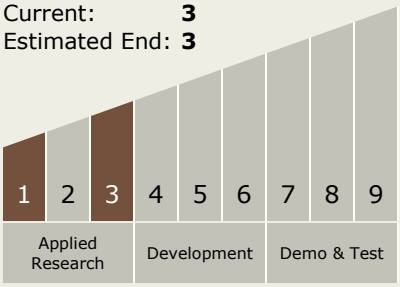
Co-Investigator:
Denis Zelenin

20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase I

Completed Technology Project (2016 - 2016)

Technology Maturity (TRL)

Start: **1**
Current: **3**
Estimated End: **3**



Technology Areas

Primary:

- TX08 Sensors and Instruments
  - TX08.1 Remote Sensing Instruments/Sensors
    - TX08.1.4 Microwave, Millimeter-, and Submillimeter-Waves

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System